WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

memory cells formed on a main surface of a semiconductor substrate, and each having first and second transistors each having a gate electrode and impurity regions forming source/drain as well as one capacitor; and

bit and word lines for controlling an operation of said memory cells, wherein

a cell plate of said capacitor is formed of the same layer as said gate electrode.

2. The semiconductor memory device according to claim 1, wherein

said cell plate is in electrical communication with the impurity region of said first transistor, and is opposed to the impurity region of said second transistor with a dielectric layer therebetween.

3. The semiconductor memory device according to claim 2, further comprising:

an interconnection layer located at the same level as said bit line, wherein

said interconnection layer has a side connected to the impurity region of said first transistor via a first plug interconnection as well as another side connected to said cell plate via a second plug interconnection.

4. The semiconductor memory device according to claim 2, further comprising:

a plug interconnection overlapping, in a plan view, with a side edge of said cell plate and a side edge of the impurity region of said first transistor, wherein

a portion of said plug interconnection overlapping with the side

edge of said cell plate is in contact with said cell plate, and a portion of said plug interconnection overlapping with the impurity region of said first transistor is in contact with the impurity region of said first transistor.

5. The semiconductor memory device according to claim 1, wherein

an insulating layer is arranged at a level lower than the impurity regions of said first and second transistors for interrupting conduction between said impurity regions and its lower side.

6. The semiconductor memory device according to claim 2, wherein

an impurity concentration of the impurity region of said second transistor opposed to said cell plate is higher than that of the other impurity region of said second transistor.

7. A semiconductor memory device comprising:

memory cells formed on a main surface of a semiconductor substrate, and each having first and second transistors each having a gate electrode and impurity regions forming source/drain as well as one capacitor; and

bit and word lines for controlling an operation of said memory cells, wherein

a cell plate of said capacitor has a belt-like form extending along said word line, and

the impurity regions of said first and second transistors are opposed to said cell plate, are continuous to each other and are located along said belt-like cell plate.

8. The semiconductor memory device according to claim 7, wherein

said cell plate is located as a layer at the same level as said word

line.

9. A semiconductor memory device comprising:

a memory cell array formed of a plurality of memory cells arranged in rows and columns, and each provided with first and second transistors having gate electrodes and impurity regions forming sources/drains as well as one capacitor, bit lines corresponding to said plurality of columns and word lines corresponding to said plurality of rows; and

a sense amplifier connected to said bit lines and used for amplifying a signal for normal access to said memory cells and refresh, wherein

said first transistor is arranged as a transistor for normal access to be used for the normal access and not to be used for the refresh access, and

said second transistor is arranged as a transistor for refresh to be used for the refresh access and not to be used for the normal access.

10. The semiconductor memory device according to claim 9, wherein

said bit lines are formed of an access bit line and a refresh bit line, said first transistor is connected to said access bit line, and said second transistor is connected to said refresh bit line.

11. The semiconductor memory device according to claim 9, wherein

said word lines are formed of an access word line and a refresh word line, said sense amplifiers include an access sense amplifier to be activated via said access word line and a refresh sense amplifier to be activated via said refresh word line, and said access sense amplifier and said refresh sense amplifier operate independently of each other.

12. The semiconductor memory device according to claim 11, wherein

said semiconductor memory device employs a background refresh system for automatically refreshing said memory cell regardless of presence and absence of a refresh signal when said access sense amplifier is operating.

13. A semiconductor memory device comprising:

a memory cell array formed of a plurality of memory cells arranged in rows and columns, and each provided with first and second transistors having gate electrodes and impurity regions forming sources/drains as well as one capacitor, bit lines corresponding to said plurality of columns and word lines corresponding to said plurality of rows; and

a sense amplifier connected to said bit lines and used for amplifying a signal for access to said memory cells and refresh, wherein

said memory cells are paired with complementary memory cells, respectively, and

said sense amplifiers are formed of a normal sense amplifier connected to said bit line coupled to said memory cell and a complementary sense amplifier connected to a complementary bit line coupled to said complementary memory cell.

14. The semiconductor memory device according to claim 13, wherein

said word lines are formed of a first word line connected to said memory cell and a second word line connected to said complementary memory cell.

15. The semiconductor memory device according to claim 14, wherein

at least one of said first and second word lines is activated to activate at least one of said sense amplifier and said complementary sense amplifier.

16. The semiconductor memory device according to claim 13,

wherein

one of the transistors in said memory cell is arranged as a transistor for normal access, the other transistor is arranged as a transistor for refresh, one of the transistors in said complementary memory cell is arranged as a transistor for normal access, and the other in said complementary memory cell is arranged as a transistor for refresh.

17. The semiconductor memory device according to claim 16, wherein

said bit lines are formed of an access bit line and a refresh bit line, said word lines are formed of an access word line and a refresh word line, said sense amplifiers are formed of an access sense amplifier and a refresh sense amplifier, said normal access transistor in the memory cell is connected to said access bit line, said refresh transistor in the memory cell is connected to said refresh bit line, said normal access transistor in the complementary memory cell is connected to said complementary access bit line, and said refresh transistor in the complementary memory cell is connected to said complementary refresh bit line.

18. The semiconductor memory device according to claim 13, further comprising:

switching control means for eliminating a complementary relationship between said memory cell and said complementary memory cell, establishing an equivalent relationship between said memory cell and said complementary memory cell, and operating both the memory cells equivalently.

19. The semiconductor memory device according to claim 18, wherein

said switching control means includes sense amplifier connection control means for eliminating said complementary relationship by changing the state of connection of said sense amplifier only to said

normal bit line to the state of connection to said normal and complementary bit lines, and changing the state of connection of said complementary sense amplifier only to said complementary bit line to the state of connection to said access bit line and said complementary access bit line different from said normal bit line and said complementary bit line.

20. A semiconductor memory device comprising:

a memory array provided with memory cells arranged in rows and columns, and each including at least one transistor having a gate electrode and impurity regions forming source/drain as well as one capacitor, bit lines corresponding to the plurality of columns and word lines corresponding to the plurality of rows:

a cell plate forming one of electrodes of said capacitor and using said impurity region as an opposite electrode; and

cell plate potential changing means for changing the potential on the cell plate.

21. The semiconductor memory device according to claim 20, wherein

said cell plate is arranged for each of said word lines.

22. The semiconductor memory device according to claim 21, wherein

said cell plate has a belt-like form extending along said word line, and

said memory array is positioned along said belt-like cell plate.

23. The semiconductor memory device according to claim 20, wherein

said cell plate potential changing means is time-varying potential changing means for correcting the potential on said cell plate varying with time due to leak of potentials in said capacitor.

24. The semiconductor memory device according to claim 23, wherein

said cell plate potential changing means can reset an amount of change effected on said cell plate when accessing the memory cell.

25. The semiconductor memory device according to claim 23, wherein

said cell plate potential changing means changes the potential on said cell plate by flowing a current through said capacitor.